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A TWOFOLD REVERSIBLE CONFIGURABLE MULTIPLIER WITH 4:2 COMPRESSOR DESIGN

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ABSTRACT:

With its applications in low-power microelectromechanical systems (CMOS) and quantum computing (quantum cost reduction), reverse logic gates have become an essential computing paradigm. Low power consumption and decreased latency are critical considerations when designing a multiplier for a wide range of applications such as digital image processing, digital signal processing, etc. We employ four 4:2 compressors in our multiplier design to lower this factor, and the switching mode of these compressors is used to alternate between the precise and approximation modes. Traditional Vedic arithmetic concepts are used to create a unique architecture for high-speed multiplication. Dual quality 4:2 reverse compressor is used in a revolutionary high speed method. Comparing these compressors' efficiency to the parameters of the current state-of-the-art approximation multipliers is done. Compared to other modes, the approximation mode has an average latency and power usage that is lower. XILINX software uses verilog as a hardware description language to synthesis and simulate this paper.

Keywords: Valves with reversible gates, compressors, and a Vedic multiplier

I.INTRODUCTION

Digital signal processors (DSP), image processors, and microprocessors all regularly use multipliers. There are just a few fields in which multipliers are employed frequently: FFT, DWT, and autocorrelation. Designing low power, high speed multipliers is necessary to lower the processing system's latency and power consumption since the switching and essential calculations performed by multipliers are higher than those performed by other datapath units.

The performance of a processor's multiplier has a significant impact on its overall speed. Increases the need for high-speed multipliers, while keeping in mind the modest space and moderate power requirements of the system at the same time

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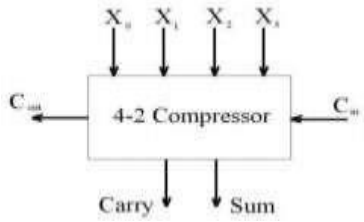
consumption. Several novel multiplier designs have been invented and investigated during the last several decades. However, the use of multipliers based on Booth's and modified Booth's algorithms in current VLSI design has its drawbacks. To get the final result, there are a number of intermediate actions that must be completed first.

The number of comparisons, additions, and subtraction operations in the multiplier and multiplicand decreases exponentially with increasing bit count in the intermediate stages. Using such designs is not a viable solution since it necessitates a number of time-consuming processes, and speed is our primary goal. In order to

A novel technique to multiplier design based on ancient Vedic mathematics was devised to

$$X_0 + X_1 + X_2 + X_3 + C_{in} = Sum + 2.(Carry + C_{out})$$



alleviate the shortcomings of the previously discussed approaches. The old and distinguished method of Vedic Mathematics serves as a basis for resolving a variety of modern-day mathematical problems. Sri Bharati Krishna Tirthaji, a well-known mathematician in India, unearthed old Vedic mathematics and brought it back to life. He divided Vedic mathematics into 16 basic sutras, making it easier for students to grasp (formulae). Many topics in mathematics and geometry are covered in these sutras. A new approach to speeding up Vedic mathematics multipliers is presented in this study, which involves replacing the current full adders and half adders with compressors. Many types of compressors are logic circuits that can add more than three bits at once instead of a full adder and can do so with a lower gate count and faster speed than an equivalent full adder circuit, making them more efficient than full adders.

COMPRESSOR STRUCTURE FOR THE TRADITIONAL 4-2

In a typical multiplier, the number of half and full adders contributes to the overall delay. Compressor structures that do more than three-bit additions are used.

Figure 1 depicts the five inputs and three outputs of the 4-2 compressor. There is no difference in the relative importance of the four inputs, one, one, two, and three as well as the output. The previous module's carry output, Cin, is passed to the following compressor, together with the current stage's carry output, Cout. what was produced Carry has a binary bit order weighting of one bit.

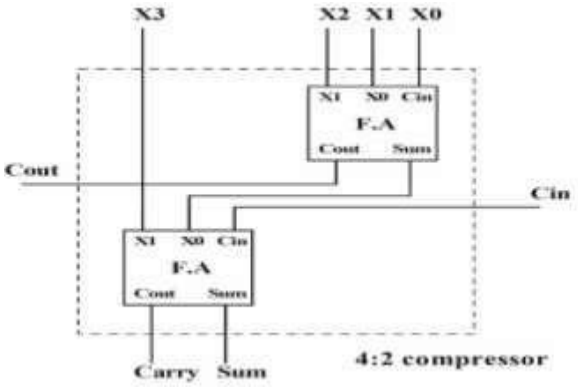
higher. The following fundamental equation governs the compressor::

Figure 1: A four-stage, two-compressor block diagram

The output Cout must be independent of the input Cin in order to speed up the carry-save summing of the partial products.

Fig. 2 depicts the traditional 4-2 compressor design, which consists of two serially coupled complete adders. A lengthy critical path delay results from a straightforward implementation of this circuit. Due to the fact that the delay

profiles of the outputs from the various inputs are all unequal.



Convential 4-2 compressor system is shown in Figure 2.

Compressors II: Dual Quality 4:2

Four dual-quality reconfigurable approximate 4:2 compressors are shown in this study.

switch between accurate and approximation modes over the course of operation. Compressors may be used in parallel multipliers with dynamic quality configuration. There are two primary components to the suggested compressors: the approximation and the additional components. Approximate mode activates just the approximate portion; accurate mode activates both the supplemental and certain components of the approximate parts. Exact and approximate modes of operation are available for the proposed DQ4:2Cs. Compressors' general block diagram is shown below..

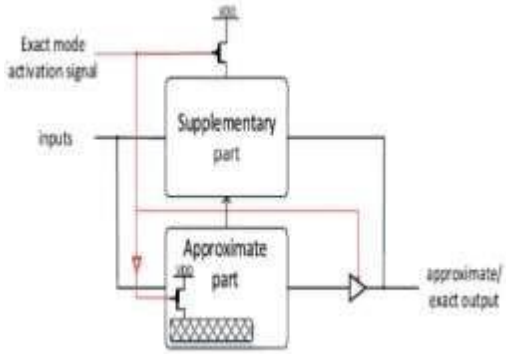


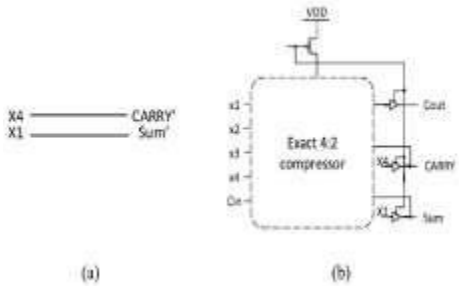
Figure 3: . a block schematic of the roughly 4:1 compressors that have been presented. An approximation part's haphazardly-drawn box identifies any components that aren't shared by this and any further parts.

Approximate and additional components make up the bulk of this diagram. It is just the approximate portion that may be used in this mode since it is power gated. The additional and partial sections of the approximate components are used in the precise functioning mode. In the suggested design, most of the components of the approximate portion are also employed during the precise working mode in order to decrease power consumption and space. We put it to good use.

a method for turning OFF the approximation part's unneeded components via the use of gating.

a. The first structure is as follows:

Using the first suggested DQ4:2C structure, as shown in Figure(a), the estimated output carry (i.e., carry) and the approximate output sum (i.e., sum) are directly coupled to the input x4 and x1 respectively. The output Cout is disregarded for the most part of this structure. This is to be expected. In spite of the structure's speed and low power



consumption, the mistake rate is high.

Approximate portion, and overall structure, of DQ4:2C1 are shown in Figure 4.

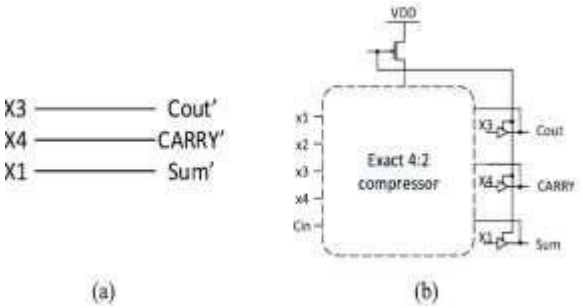
An identical 4:2 compressor completes the design as an add-on component. Figure depicts

the planned structure as a whole (b). This structure's delay is almost the same as that of a 4:2 compressor in the precise operating mode.

DQ4:2C2: a. The second structure

Even though Cout reduced the internal structure of the reduction step of the multiplication in the first structure, the error was substantial in that case. Cout The output Cout is created straight from the DQ4:2C1 in the second structure, as opposed to the DQ4:2C1.

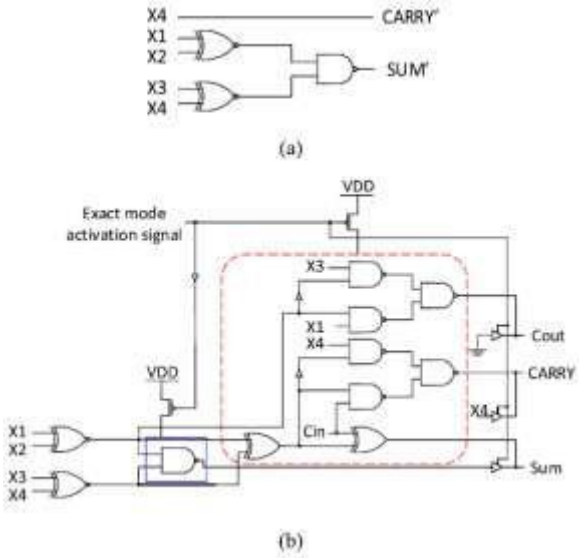
In the approximate portion, enter x3. DQ4:2C2's internal structure and overall structure are shown in Figure. This structure has the same error rate as DQ4:2C1, but its relative error is lower.



A portion of DQ4:2C2 is shown in (a) and the complete structure is shown in (b) in Figure 5.

Structure three (DQ4:2C3):

In the approximate mode of operation, the prior structures reduced power and delay to their maximum levels as compared to the precise compressor. A greater level of precision may be required in specific cases. This structure's internal structure, given in Figure, shows how increasing the complexity of the approximation section improves the approximate operating mode's accuracy (a). The output sum's precision is improved with this arrangement. Like DQ4:2C1, the approximate portion of this Structure does not allow Cout output. However, compared to earlier structures, this one has a lower mistake rate.

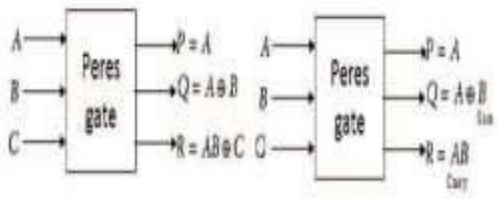


A portion of DQ4:2C3 and the overall structure of DQ4:2C3 are shown in Figure 6.

Figure (b) shows the overall structure of DQ4:2C3 with the supplemental section contained in a red dashed line rectangle. A blue dotted line rectangle indicates that the NAND gate used in the approximate component is not employed in the precise operating mode of this arrangement. Because of this, we recommend turning off the gate's power supply voltage while in this mode of operation.

a. Structure 4 (DQ4:2C4):

Compared to DQ4:2C3, the output carry accuracy in this structure is improved at the expense of a bigger delay and higher power consumption when the error rate is lowered more. Fig. 7 illustrates the internal structure of the approximation component and the overall structure of DQ4:2C4. Gates of the approximate portion, which are powered OFF during the precise operating mode, are marked by a blue dotted line. The additional part is denoted by a red dashed rectangle line.



DQ4:2C4's overall structure is shown in Figure 7(a).

II. THE DESIGN OF THE SYSTEM Constructive Reversal:

Due to its potential to decrease power consumption, reversible logic has been more relevant in the design of low-power VLSI circuits in recent years. It uses a physical process that is both thermodynamically and conceptually reversible, based on quantum computing. At least kTln2 joules of energy are required for each irreversible bit operation, according to Landauer's study. k=1.3806505*10-23m2kg-2K-1(joule/Kelvin-1) joules. There must be a one-to-one relationship between an electronic circuit's input and output if it is stated to be reversible. It is utilized in this research to create 4:2 compressors using a standard 4x4 input TSG gate. Peres gates and TSG gates are the most basic gates utilized in this study.

The Peres gate as an adder is shown in Figures 8(a) and 8(b).

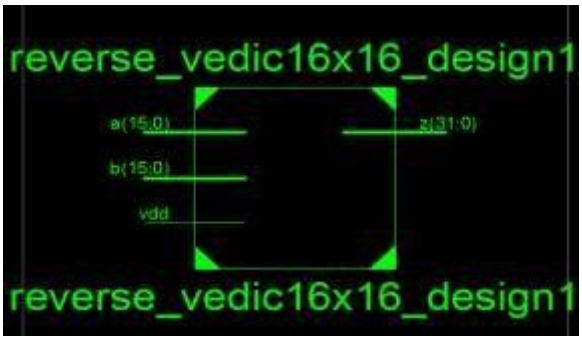
The entrance at Peres's Gate Figure b depicts a Peres gate with a 3*3 configuration. (A, B, C) is the input matrices, while (O) is the output matrices (P, Q, and R). P = A, Q = A is the output.

In this case, B and R = (A.B. C). A Peres gate's quantum cost is four.

Final adders aren't necessary since the compressors' output already yields FinalProduct in the approach under consideration. To put it another way, as compared to ordinary multipliers, the circuit's complexity has been greatly reduced. The same parameter is determined using logical calculations, and it was discovered that the vedic multiplier uses less computations.

II. RESULTS

Using reversible gates like peers gate, TG gate, and 4:2 compressors, an unique Vedic multiplier is created in this part by applying the reversible notion to the adder.



Designs	Dadda multiplier		Reverse vedic multiplier	
	Number of LUT's	Delay	Number of LUT's	Delay
Multiplier 1	124	6.274 ns	109	6.823 ns
Multiplier 2	127	6.080 ns	111	6.833 ns
Multiplier 3	145	5.736 ns	115	6.840 ns
Multiplier 4	158	6.925 ns	124	8.024 ns

Table 1: Comparision of multiplier designs

II. CONCLUSION:

Compressor-based Vedic multipliers employing reversible logic are described in this study as four DQ4:2Cs.

The ability to switch between accurate and approximate modes of operation. Accuracy was sacrificed for faster speeds and reduced power usage in the approximate mode of these compressors. It's important to note that the approximate and accurate modes of these compressors each had a distinct degree of precision, as well as differing delays and power

in the approximate mode. Using these compressors, an 8-bit multiplier was able to give a dynamically programmable multiplier with variable accuracy, power, and speed.

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